CLAIMS

1-18 (Cancelled).

19. (Previously presented) A selectable frame synchronization structure transmission repeater comprising:

a repeater input port to accept a first stream of information including a first arrangement of synchronization bits; and

a decoder having a first input connected to the repeater input port to receive the first stream of information, the decoder reading the first arrangement of synchronization bits to organize the first stream of information into a first frame structure including a data section and a header section having a plurality of *m* bits, the decoder having a second input for selecting the first arrangement of synchronization bits to be read by selecting a number of synchronization bits in the range from zero to *m* bits, selecting the bit position of the synchronization bits in the header section, and selecting the content of each synchronization bit in the header section.

20-22. (Canceled).

23. (Previously presented) The repeater of claim 19 further comprising:

a deinterleaver circuit having an input to receive the first stream of information, the deinterleaver circuit deinterleaving the first stream of information into a plurality of *n* parallel data streams; and

in which the decoder's first input includes a plurality of *n* inputs connected to the deinterleaver to receive the first stream of information in *n* parallel data streams, the decoder's selection of the first arrangement of synchronization bits includes selecting an arrangement of synchronization bits in each of the *n* parallel data streams to form a first frame structure including header and data sections in each data stream.

24. (Original) The repeater of claim 23 in which the decoder's selection of the first arrangement of overhead bits includes selecting independent arrangements of synchronization bits for each header section of the *n* parallel data streams.

25. (Previously presented) The repeater of claim 24 in which the deinterleaver circuit deinterleaves the first stream of information into four parallel data streams; and

in which the decoder's selection of the first arrangement of synchronization bits includes reading a first group of bits from the first parallel data stream header section, reading a second group of bits from the second parallel data stream header section, reading a third group of bits from the third parallel data stream header section, and reading a fourth group of bits from the fourth parallel data stream header section.

26. (Previously presented) The repeater of claim 19 further comprising:

an encoder having an output to provide a second stream of information organized in the first frame structure with header sections, the encoder having an input for selecting a second arrangement of synchronization bits to be written in the header section; and

a repeater output connected to the encoder output to provide the second stream of information.

27. (Original) The repeater of claim 26 in which the encoder organizes the second stream of information into a plurality of *n* parallel data streams, and in which the encoder selection of the second arrangement of synchronization bits includes selecting the synchronization bits to be written in the header sections of the *n* parallel data streams, the encoder having a plurality of *n* outputs to provide the *n* data streams; and

further comprising:

an interleaver circuit having a plurality of *n* inputs connected to *n* encoder outputs, the interleaver circuit interleaving the parallel data streams in to the second stream of information, the interleaver circuit having an output connected to the repeater output.

28. (Previously presented) The repeater of claim 19 in which the repeater input receives the first stream of information in a protocol selected from the group consisting of datacom, telecom, fiber channel, SONET, SDH, and Gigabit Ethernet protocols.

29. (Previously presented) A selectable frame synchronization structure communication system comprising:

a transmitter having an output to provide a first stream of information in a first frame structure with a header including a first arrangement of synchronization bits of the first stream of information;

a repeater including:

a repeater input port to accept the first stream of information; and

a decoder having a first input connected to the repeater input port to receive the first stream of information, the decoder reading the first arrangement of synchronization bits to organize the first stream of information into the first frame structure including a header section, the decoder having a second input to select the first arrangement of synchronization bits to be read;

an encoder having an output to provide a second stream of information organized in the first frame structure with a header section, the encoder having an input for selecting a second arrangement of synchronization bits to be written in the header section; and

a repeater output connected to the encoder output to provide the second stream of information.

30. (Canceled)

31. (Previously presented) The system of claim 29 further comprising:

a receiver having an input connected to the repeater output to accept the second stream of information, the receiver reading the second arrangement of synchronization bits to organize the second stream of information [stream] into the first frame structure.